GaAs MESFET Physical Models for Process-Oriented Design

Christopher M. Snowden, *Senior Member, IEEE,* and Renato R. Pantoja

***Abstract*—A detailed physical model is described which is used to accurately predict the dc and microwave performance of GaAs MESFET's. This model, which accounts for hot electron effects in sub-micron FET's, includes trapping phenomena and heating due to power dissipation. It is used to determine the optimal design for small-signal and power devices, including single- and double-recessed FET's. The spread in device characteristics can be directly related to the variation in device geometry and process parameters experienced in fabrication. The accuracy and flexibility of this approach is demonstrated by comparison with measured data for a variety of devices.**

I. Introduction

THE DESIGN and characterization of microwave devices and circuits has traditionally relied on utilizing measured small-signal *S*-parameter and dc data which is frequently used in association with equivalent circuits, where the element values are obtained by fitting the model terminal characteristics to the measured data. This approach is largely empirical and requires extensive experimental data to establish a good basis for design and is particularly demanding in the case of devices operating in non-linear circuits, such as power amplifiers and oscillators. In these circumstances, measured data is required for a wide range of dc bias levels, signal amplitudes and frequencies, because of the nonlinearities of the active device. In addition to the constraints imposed by the operating conditions of the device, other phenomena have a significant impact on the characterization of microwave transistors. For example, trapping phenomena associated with III-V transistors are known to degrade the large-signal performance of power FET's and it is very difficult to characterize this effect with equivalent circuit models. Furthermore, the development of new FET-based designs usually requires many costly and time-consuming fabrication-design iterations, because of the difficulty in relating device geometry and doping profile to the equivalent circuit element values. Thermal effects in active devices can have significant impact on the design and operation of circuits. In particular, in the case of design methods based on equivalent circuit models derived from measurements, if the thermal environment of the prototype circuit differs from that present during the characterization, the final circuit performance may deviate from the expected design values.

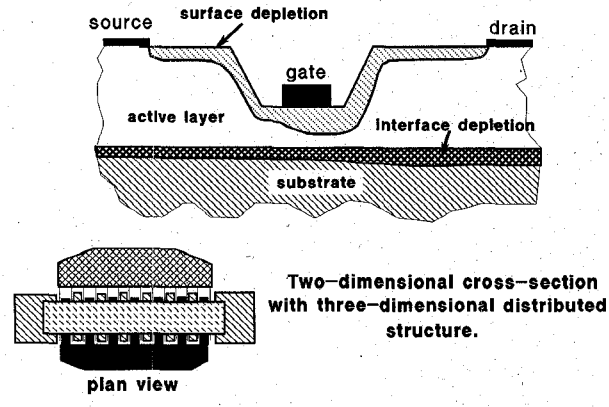


Fig. 1. Schematic cross-section and plan view of a MESFET with a single gate-recess.

This paper presents an alternative approach for microwave FET characterization and design, based on a highly efficient physical model. This model accounts for carrier transport in the active channel (two-dimensional cross-section) and for the distributed (three-dimensional) nature of the FET structure [1], [2], Fig. 1. The physical device model used in this work is intrinsically capable of simulating dc, small- and large-signal operation, without making any successive modifications to the model. The model presented can be used to *predict* the operation of new devices with confidence prior to fabrication, and allows *both* the device and circuit to be optimized for a particular application. This makes the design of new devices systematic (and quantitative), minimizing uncertainty in the design due to doping profile and process requirements. This type of model can be used to predict parameter spreads and yields prior to fabrication, since the device geometry and material parameters, which play a major role determining spreads and yields, form the basis of the model. This paper deals with the development and application of a physical FET model suitable for predicting dc and microwave small- and large-signal characteristics, and demonstrates its accuracy and speed compatibility with current microwave CAD practice. The physical model described in this paper accounts for thermal effects due to power dissipation and variable ambient temperature. A key feature of this approach is that it is possible to relate

Manuscript received November 8, 1991; revised January 13, 1992.

C. M. Snowden is with the Microwave Solid State Group, Department of Electronic and Electrical Engineering, University of Leeds, Leeds, LS2 9JT, UK.

R. R. Pantoja is with M/A-COM Inc., Corporate Research and Development Center, 52 South Avenue, Burlington, MA 01803.

IEEE Log Number 9108314.

physical and geometrical changes in the device design to changes in the performance. In particular, this model allows a wide range of design and process parameter variations to be investigated in a very short period of time without resorting to fabrication experiments. This approach can be used to obtain a more cost-effective and speedy solution for obtaining the optimum design and maximizing the yield of both small-signal and power FET's.

II. The Physical Model

In contrast to equivalent circuit models which can be used to reverse-model devices using measured data, physical models are essentially predictive, producing results based on the physical geometry and description of the device and circuit. This type of model is *not* obtained by fitting model parameters to measured electrical data as in equivalent circuits and semi-empirical physics-based models, and hence the quality of agreement between measured and simulated results is mainly a function of the quality and accuracy of process data supplied to the model, assuming that the physics and parasitics are adequately described. In the case of sub-micron gate length MESFET's this implies that a model capable of representing hot electron effects is required. There have been many contributions of full two-dimensional modelling of GaAs MESFET's, the more recent of which address the issue of CAD and optimization [3], [4]. However, these comprehensive two-dimensional models are too computationally intensive for present resources, preventing interactive design and analysis. Quasi-two-dimensional models [1], [5], [6], [7], [8] retain the essential physical description, but allow several orders of magnitude improvement in speed [1], [2].

The quasi-two-dimensional model used in this work incorporates a hot electron model solving both energy and momentum conservation equations. The basic principles of this model are described elsewhere [1], [2]. The model presented in this paper has been substantially improved incorporating a charge-control model, improved doping profile description, a thermal dissipation model, improved surface and substrate trap representation and a more flexible cross-sectional geometry description. The semiconductor transport equations are solved in a highly efficient quasi-two-dimensional manner [1], retaining a two-dimensional description of the active channel, Fig. 2, but only requiring a numerical solution of the x-component of the electric field. The electron transport equations for this model are,

$$\frac{\partial EY}{\partial x} = \frac{q}{\epsilon_0 \epsilon_r}\left[\int_{Y_D}^{\infty} (N_D - N_A + N_{DT} - N_{AT})\, dy - \int_{Y_D}^{\infty} n\, dy\right] \quad \text{Poisson's Equation} \tag{1}$$

$$i_S = i_{ch}(x) + i_g(x) + i_{\text{aval}}(x) \quad \text{current continuity} \tag{2}$$

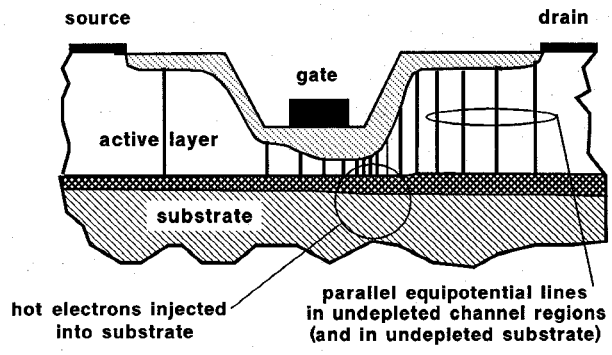


Fig. 2. Quasi-two-dimensional approximation for a MESFET, showing parallel equipotential lines in the undepleted active channel.

$$v = \mu(w, T_0)\left(E - \frac{2}{3}k_1(w)\frac{dw}{dx} - \frac{k_2}{n}\frac{dn}{dx}\right]$$

momentum continuity (3)

$$\frac{dw}{dx} = \frac{1}{1 + \frac{2}{3}K(w)}\left(E - \frac{w - w_0}{v\tau_w(w)}\right)$$

energy conservation (4)

where E electric field, w average electron energy, n electron density, v electron velocity, i_S, $i_{ch}(x)$, $i_g(x)$, $i_{\text{aval}}(x)$ are the source, channel, gate and avalanche multiplication currents. Y_D is the edge of the Schottky depletion region, q magnitude of the charge on the electron and $\epsilon_0\epsilon_r$ is the permittivity of the material, K, $k_1(w)$ and k_2 are multivalley transport parameters [1], τ_w is the energy relaxation time and w_0 is the equilibrium energy corresponding to the lattice temperature T_0. N_{TD} and N_{TA} are the ionized donor and acceptor trap densities. μ is the electron mobility which is a function of average electron energy w and lattice temperature T_0.

It should be noted that (1) differs from previously published work [1], fully accounting for both the doping profile (donor and acceptor) and for variable trap density. The Poisson, energy and momentum continuity equations are solved using a finite-difference numerical scheme. The source current i_s and gate voltage v_G are used as boundary conditions, from which the drain voltage v_{DS} is determined. The solution of these equations yields the terminal voltage and current responses.

The model, which already accounts for breakdown and gate conduction [1], has been substantially improved with new semi-insulating substrate and doping profile descriptions and optional n+ implant regions. This improved model allows both single and double-recessed FET structures appropriate for contemporary power FET designs to be simulated, Fig. 3. The model has shown that the electric field and electron energy distributions of double-recessed designs are significantly different from those of single-recessed FET's, with associated reduction in peak electric field below the drain edge of the gate, accounting for the improved breakdown characteristics of the former. The breakdown characteristics and microwave performance of double-recessed FET's are a strong function of

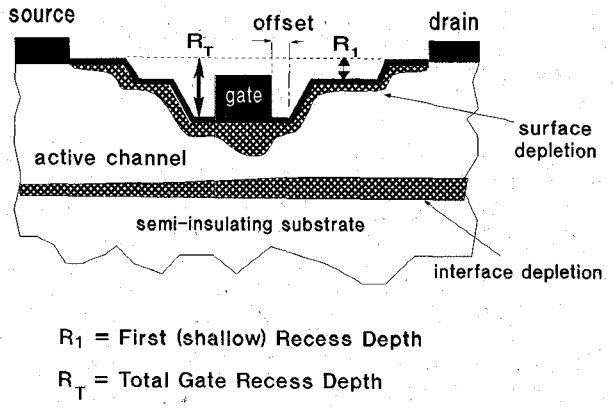


Fig. 3. Double-recessed gate power FET structure. R_I = first (shallow) recess, R_T = total gate recess.

the doping profile and surface state density. Another consequence of the double-recessed gate structure and the reduction in peak electric field, is that the effective gate length is increased with the charge-dipole extending towards the drain, decreasing the f_T of the device and lowering the transconductance compared with single-recessed devices.

Heat dissipation in microwave devices can substantially modify both the dc and microwave characteristics. This FET model has had a simple thermal model incorporated, where the average lattice temperature T_0 is calculated as a function of dissipated power and thermal resistance. This temperature is then used to determine the energy-dependent mobility by relating temperature dependent steady-state velocity v_{ss} (given in [9]) to the equivalent steady-state electric field E_{ss}, which is in turn extracted from an energy-electric field characteristic obtained from Monte-Carlo simulations (as in [1]). This yields the mobility as,

$$\mu(w, T_0) = \frac{v_{ss}(E_{ss}, T_0)}{E_{ss}(w)} \, m^2 vs^{-1}$$

where

$$v_{ss} = \frac{300\mu_0}{T_0} E_{ss} \left[\frac{1 + \dfrac{8.5 \times 10^4 E_{ss}^3}{\mu_0 E_0^4 (1 - 5.3 \times 10^{-4} T_0)}}{\left(1 + \left[\dfrac{E_{ss}}{E_0}\right]^4\right)} \right] ms^{-1} \tag{5}$$

where μ_0 is the average low field mobility of the active channel obtained by mobility profiling) and E_0 is the characteristic field 4×10^5 Vm^{-1}. The average lattice temperature is obtained using

$$T_0 = T_{\mathrm{amb}} + P_D R_{TH} \tag{6}$$

where T_{amb} is the ambient temperature of the mounting surface, P_D is the power dissipated in the device (power from the supply-signal power) and R_{TH} is the total thermal resistance between the active region of the device and the mounting surface/heatsink. In the absence of a signal (or for small-signal conditions) the dissipated power is determined from the product of the bias voltage and current $V_{DS}I_D$. R_{TH} was typically found to lie in the region of 70°C/W for 300 micron wide FET's measured using wafer-probe techniques. The thermal impedance of larger devices has been investigated using separate thermal modelling software [10]. The application of the thermal model requires an iterative solution, since the bias point is a function of temperature and the temperature itself is itself a function of bias (dissipated power). DC solutions using this thermal model typically require 4 or 5 iterations to converge. The quasi-two-dimensional model has the advantage of retaining a relatively rapid solution (typically 1.5 s per bias point on an IBM PC) compared with full two-dimensional models which are prohibitively slow. It should be noted that pulsed simulations (for transient I–V characterization) do not require the use of a thermal model and are significantly faster.

The observed differences between steady-state dc and pulsed (fast transient) I–V characteristics and low frequency dispersion associated with g_m and g_d are attributable to the dynamic behavior of deep level traps in the bulk material and at the surface of GaAs MESFET's [11]–[13], Fig. 4. Deep level traps are due to both unwanted impurities such as carbon (associated with the EL2 level), and to intentional doping with chromium. The impact of bulk traps is particularly significant for ion-implanted FET's, but time-dependent behavior of surface traps remains important for both epitaxial and ion-implanted devices. The filling of these traps is dependent on their concentration, capture cross-section, position in the energy band-gap and on the carrier distribution in the channel and substrate. Acceptor sites are ionized when the trap energy level is below the Fermi level, whilst donor centers are ionized when the trap level is above the energy level. The improved quasi-two-dimensional model accounts for the behavior of substrate and surface trapping phenomena which enhance the accuracy of the model, particularly in the case of ion-implanted FET's (where the channel-substrate barrier and trap influence is more completely accounted for than in earlier models). These effects are also intrinsically accounted for when microwave operation is considered. A charge-control model has been implemented to improve the accuracy in calculating the depth and charge associated with the gate and surface depletion regions. Earlier models had difficulty representing device operation close to pinch-off because of the use of simplifying uniform doping density and the absence of a channel-substrate interface description [1], [14]. This problem has been overcome using the new charge-control model.

A. Charge-Control Model

This quasi-two-dimensional simulation originally described in [1], has been modified to include a charge-control model to determine the charge in the depletion region, charge in the channel and depletion depth as a function of

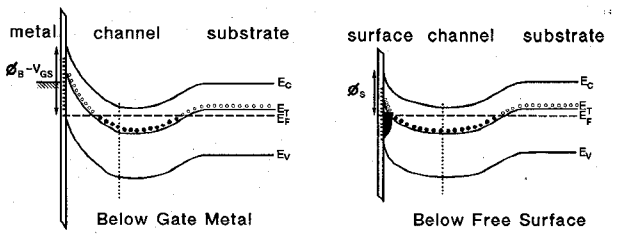


Fig. 4. Energy-band structure of GaAs MESFET (i) below gate (ii) below free surface. E_F is the Fermi Level, E_C is the conduction band energy, E_V is the valence band energy and E_T is the deep level trap energy.

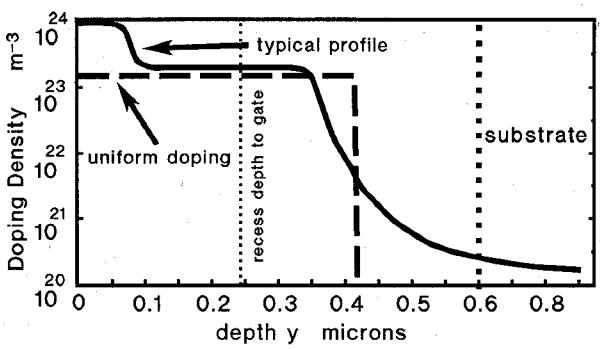


Fig. 5. Doping profile of a typical MESFET with the equivalent doping profile [14].

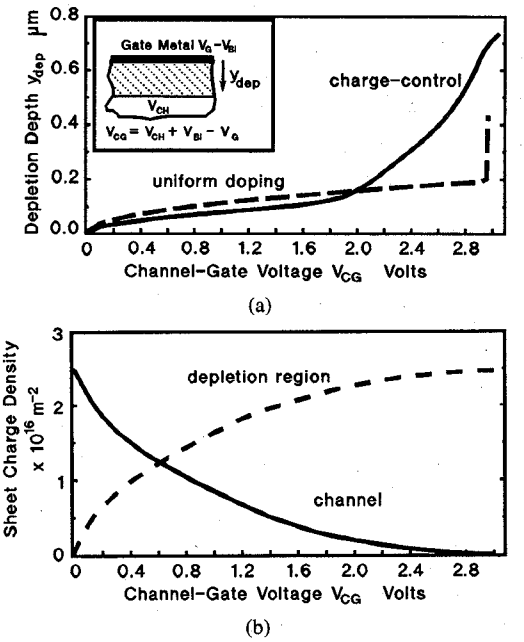


Fig. 6. Charge-control characteristics for the profiles in Fig. 5. (a) Gate depletion depth as a function of channel-gate voltage (b) charge associated with the conducting active channel and gate depletion region (for the typical profile).

channel to gate potential V_{CG} at each point in the channel. This allows the doping profile and influence of traps to be accounted for, achieving superior accuracy to that of earlier models [1], [14]. Carrier-profile models accounting for deep-levels have been previously described [15] and a similar approach is taken here to develop a charge-control model for the FET incorporating both deep levels and surface states. The Poisson equation (1) is solved to obtain the potential V_{CG} with respect to the surface, as a function of depth through the profile. This involves determining the trap filling for each bias condition (channel-gate), to determine the ionized donor and acceptor densities. In order to simplify the solution, it is assumed that there is zero gate current in reverse-bias. The Poisson equation is solved by performing a numerical double integration of the total charge shown on the r.h.s. of (1), using a Simpson integration technique. This is performed for steady-state case, assuming that the traps reach equilibrium for each gate-channel bias and for a transient case (assuming $\tau < 1$ ns), where the traps do not respond (V_{CG} is rapidly 'pulsed' from 0 V). This yields two separate the charge-control characteristics for steady-state dc simulations and for microwave simulations (including S parameters).

The application of the charge-control model is illustrated in Figs. 5 and 6. Fig. 5 shows a typical epitaxial doping profile for a MESFET together with a commonly used equivalent uniform doping representation, as in [14] (with the same pinch-off voltage and maximum current I_F). The position of the gate recess and substrate are marked. Fig. 6 shows the resulting characteristics of the charge-control model obtained from these profiles. Although the depletion depth function in Fig. 6(a) tracks reasonably closely for both profiles for a large part of the channel-gate voltage range, a significant difference occurs approaching the pinch-off voltage V_{PO} (2.9 V). The charge-control model for the true profile allows the pinch-off of the device to be more closely followed and takes account of the profile tail and substrate interface, whereas the uniform doping approximation produces an unrealistic result close to pinch-off. It is important to appreciate here that in the absence of a suitable substrate model, which accounts for the presence of traps, the depletion depth would sharply tend towards full thickness of the substrate for values of V_{CG} greater than V_{PO}. The presence of traps ensures that the depletion depth increases in a well behaved manner, although the rate of change of depletion depth with V_{CG} increases sharply when the highly doped active channel and channel-substrate interface are fully depleted.

The charge-control relationship is obtained at the start of the simulation, requiring in the region of 25 CPU seconds on a 20 MHz 386 PC. The use of this type of charge-control model, together with a non-uniform finite-difference mesh, allows the transport equations to be solved extremely efficiently, typically requiring less than 0.3 CPU seconds per solution on the same personal computer (this increases to 1.5 CPU seconds for simulations including the thermal model).

The physical model is used to extract dc characteristics, time-domain microwave responses (for S parameters and large-signal simulations), quasi-static bias-dependent equivalent circuit elements and for simple circuit simulation. The basic techniques for applying this model is described in [1] and [2]. This paper will demonstrate the application of this model to both small-signal and power

FET's, concentrating on how the model can be used to *predict* the dependence of dc and microwave performance on geometrical and fabrication parameters. This is turn can be used to predict the dependence of yield on the fabrication process.

III. Application and Results

The main purpose of this model is for use in CAD of devices and circuits and the relatively short execution times, typically less than 2 min for predicting a complete dc characterization and a full set of quasi-static bias-dependent equivalent circuit model elements at 150 bias points, on a 20 MHz 386 desk-top personal computer, makes this approach an attractive alternative to traditional equivalent circuit models. S parameters typically require 2 min per frequency for a full c.w. time domain and bias-dependent simulation on the same computer. It should be noted that it has been found that a time-domain cw extraction of bias-dependent S-parameters is more accurate than the commonly used transient simulation technique (as first described in [16] for FET's). Although a frequency-domain solution of the linearized quasi-two-dimensional equations would yield similar small-signal accuracy with increased efficiency, the generalized time-domain technique used here is also suitable for representing highly nonlinear operation, discussed in Section III.

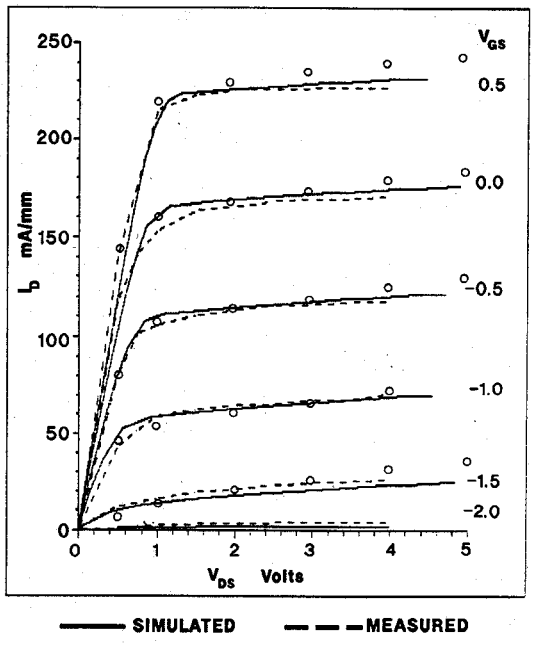
It is well known that the geometrical and physical parameters associated with microwave devices are subject to spreads during fabrication. It is common to find variations in gate length and recess depth of the order of 15%, with variations in gate offset in a recess of up to 0.1 microns (the distance between the gate metal and the edge of the recess if present). The control over the doping profile has improved significantly in recent years, but variations between batches of wafers are still to be expected. In particular, the mobility for ion-implanted layers may vary by 20% from batch to batch. The model presented in this paper allows the effects of these variations to be directly related to dc and microwave performance, by carrying out a number of simulations incorporating the observed range of process parameter spreads.

In order to determine the absolute accuracy of the model, a number of specific MESFET's were simulated, where the geometrical and physical parameters of the devices were carefully identified. This was done with the aid of cross-section SEM data, mobility profiling of material samples close to the devices, and careful process characterization. It is important to appreciate that all of the following results are obtained directly from the physical model, using the available physical data on the FET, *without* any additional fitting. The RF results can be improved to achieve an excellent level of 'fit' by adjusting the passive parasitic element values, but this was not the aim of the work, which was to demonstrate the predictive capability of the simulator.

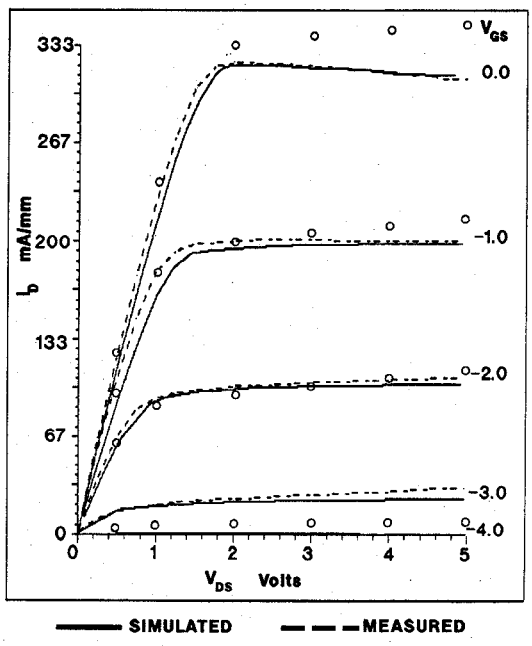
A specific epitaxial 0.5 micron gate length MESFET was simulated under pulsed conditions to illustrate the transient capability of the model. In these circumstances it is assumed that the traps do not respond within the timescale of the pulse, and thermal dissipation is negligible. The simulated results are compared with pulsed wafer-probe measurements in Fig. 7(a). The agreement is good both in terms of absolute value and the slope of the characteristics (confirming accurate modelling of g_d and g_m). The improvement in the quality of results obtained for pulsed I–V analysis using the improved model compared with the earlier model [1] is illustrated in Fig. 7(a). It is evident that both the slope of the characteristics and the dc values themselves are in closer agreement with measured data for the new model. This is attributable to the charge-control model which also accounts for the real doping profile and the influence of traps. A specific 1 micron gate-length ion-implanted device, with a double implantation used to produce an n^+-n profile, and a shallow single gate-recess, was simulated over a range of dc bias conditions, (where the traps have attained their steady-state). The results for this device are shown in Fig. 7(b), where they are compared with wafer-probed dc measurements. Again the agreement is very good for this selected device, and the relatively simple thermal model appears to represent heating effects in this device adequately (the dc results from the original model [1] which also did not account for heat dissipation are shown for comparison). The result is even more significant for ion-implanted FET's.

A comparison between simulated and measured S parameters for the 0.5 micron and 1 micron gate length FET's is shown in Figs. 8 and 9. The measured data was obtained using wafer-probe techniques. The particular significance of these results is that they were obtained directly as a result of applying the physical model and process data, *without* any fitting to measured data or reverse-modeling. The model makes use of only the parasitics calculated during the simulation from the physical data, which includes the contact resistances, interelectrode capacitances and distributed nature of the gate.

The breakdown characteristics of FET's intended for power applications are particularly important. The model includes the breakdown mechanisms associated with the channel and surface (incorporated into i_{aval} in (2)) [1], [17]. The correlation between measured and simulated breakdown voltage V_{DGB} as a function of saturated drain current I_{DSS} for the 1 micron gate length FET is shown in Fig. 10. The measured results were obtained from experiments aimed at investigating the influence of the fabrication process on device performance. The range of simulation data accounts for variation in gate recess depth (20%), gate metal offset in the recess (0 to 0.1 microns) and variation in mobility across the samples (15%). The combination of results obtained from simulations including these variations forms the range of predicted results shown in Fig. 10. The impact of gate offset on the dc characteristics is relatively small in this MESFET because of the very shallow recess. The range of simulated data generally agrees well with the range of measured re-



(a)



(b)

Fig. 7. Measured and simulated I–V characteristics for specific FET's. (a) pulsed I–V characteristics for a 0.5 micron gate length epitaxial MESFET (short-pulse conditions). (b) DC characteristics for a 1 micron gate length ion-implanted MESFET (——— new model, ○○ old model, ---- measured data).

sults indicating that this is a useful way of assessing the variation in device performance.

MESFET's employing a double-recessed gate are a popular choice for power transistor designs, Fig. 3. However, the expected behavior of double-recessed gate FET's can depart significantly from the single-recessed counterparts. An investigation of the influence of the relative recess depths in double recessed FET's has been carried out for epitaxial power FET's and some results obtained using the new model are presented here. The simulated de-

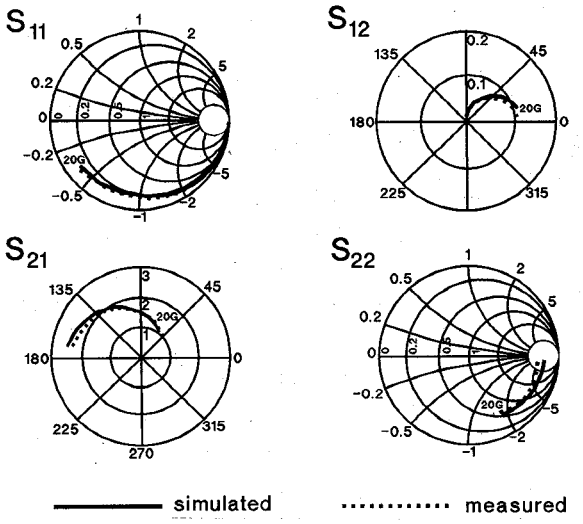


Fig. 8. Comparison of measured and simulated S-parameters for a specific 1 micron gate length ion-implanted MESFET, 1 to 20 GHz (——— simulated, ---- wafer probed measured data). $V_{DS} = 4$ V, $V_{GS} = -1.4$ V.

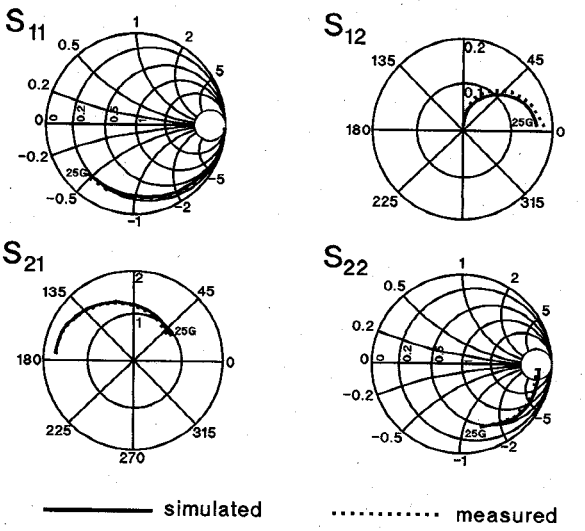


Fig. 9. Comparison of measured and simulated S-parameters for a specific 0.5 micron gate length epitaxial MESFET, 1 to 25 GHz (——— simulated, ---- wafer-probed measured data). $V_{DS} = 4$ V, $V_{GS} = -1.0$ V.

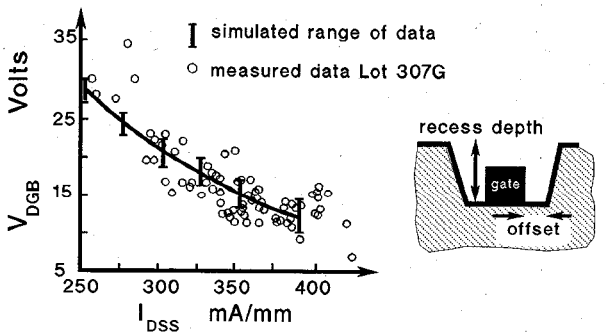


Fig. 10. Variation in breakdown voltage V_{DGB} with I_{DSS} for 1 micron gate length ion-implanted power FET (I simulated range of data, ○ measured FET's).

pendence of V_{DGB}, I_{DSS}, f_T and maximum output power P_O (optimized resistive load at each point) on the ratio of the first recess to the total gate recess depth R_1/R_T is shown

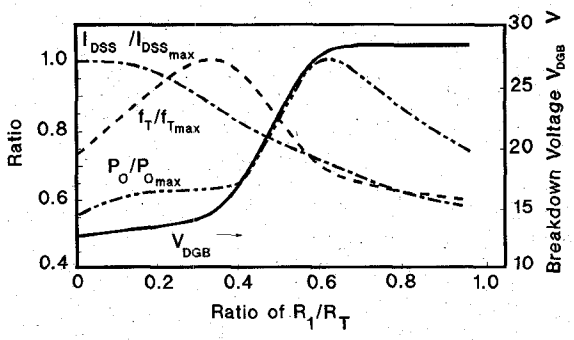


Fig. 11. Simulated dependence of V_{DGB}, f_T, $P_{O\max}$, I_{DSS} of an epitaxial double-recessed gate FET as a function of the ratio of recess depths $R_l:R_T$. (f_T, $P_{O\max}$, I_{DSS} are normalized to their maximum values).

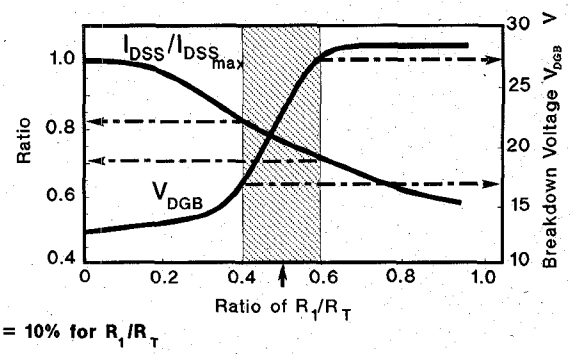


Fig. 12. Spread in I_{DSS} and V_{DGB} due to the variation in ratio of recess depths $R_l:R_T$ encountered in fabrication for σ of 10% in $R_l:R_T$, centered at a ratio of 0.5.

in Fig. 11. This important result clearly illustrates the sensitivity of the FET performance to this ratio and it is believed to be the first time a physical model has been used to investigate the performance of double-recessed power FET's. Although the double-recess structure allows greater breakdown voltages to be achieved, variation in the relative ratio of the recess depths across the wafer leads to further spreads in the dc and microwave parameters. When the ratio of recesses is close to 0.5, measured V_{DGB} values were between 17 and 26 V across a wafer, with an average of 23 V (σ = 10%), which compares well with the predicted performance in Fig. 12 and Table I. Power densities of greater than 600 mW/mm and efficiencies above 40% at 8 GHz have been obtained from this FET design. This diagram also shows the trade-off between V_{DGB}, P_O and f_T, for this particular double-recessed power FET structure.

The correlation between breakdown voltage V_{DGB} and I_{DSS} for the double-recessed design is shown in Fig. 13. Here the total variation in simulated device performance is shown for typical variations in recess depth, ratio R_l/R_T and gate offset associated with this process. Average values obtained from measurements of power FET's for each wafer from 23 wafers are shown for comparison. The apparently large variation in both predicted and measured results can be attributed to the sensitivity to both recess depth and offset of the gate metallization in the recess. In particular, the relatively large offset associated with gates deposited in deep recesses degrades V_{DGB}, f_T and I_{DSS}. It is also very important to appreciate that the strong nonlinear dependence of these parameters on the ratio R_l/R_T illustrated in Fig. 13, implies that analysis based on statistical averages may not provide a consistent comparison with simulated data because of the nonuniform distribution. For example, a small shift in the average value of the ratio R_l/R_T from 0.5 to 0.4 significantly decreases the average breakdown voltage from 23.5 V to 17 V. This type of variation may account for some of the differences between the simulated and measured range of data observed in Fig. 13.

The model can be readily applied to the large-signal characterization of MESFET's. This is achieved using the modified harmonic balance technique described in [2].

TABLE I
SPREAD IN I_{DSS} AND V_{DGB} DUE TO THE VARIATION IN RATIO OF RECESS DEPTHS $R_l:R_T$ ENCOUNTERED IN FABRICATION FOR σ OF 10% IN $R_l:R_T$, CENTERED AT A RATIO OF 0.5

	Simulated		Measured	
	Range	Mean	Range	Mean
I_{DSS} mA	238–312	280	229–308	276
V_{DGB} V	16–27	23.5	17–26	23

σ = 10% for R_l/R_T (Results for One Wafer).

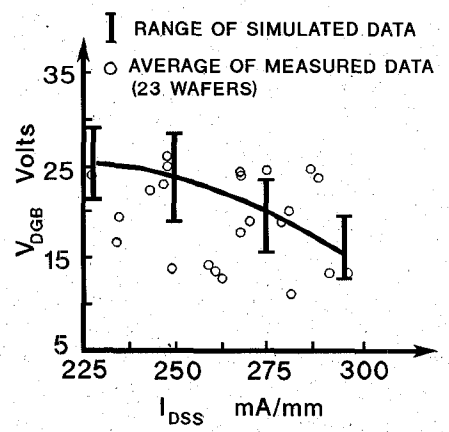


Fig. 13. Variation in breakdown voltage V_{DGB} as a function of I_{DSS} for the 0.5 micron gate length epitaxial double-recessed gate power MESFET (I simulated range, ○ average of measured data for each wafer).

This algorithm has been improved to increase the speed of convergence. The modified harmonic balance method is not based on derivative information and hence does not utilize Jacobians. This method is highly efficient for mildly nonlinear operation, but converges satisfactorily even at high drive levels (well in excess of 3 dB gain compression). For example, at the 3 dB compression point, the simulator typically requires in the region of 150 iterations, taking 30 s on a 20 MHz IBM PC. The large-signal simulation can be achieved using either the physical model or a non-linear self-consistent (charge-conservative) quasi-static equivalent circuit model derived using the physical model [2]. The latter approach is significantly faster than the physical model, but is limited by the

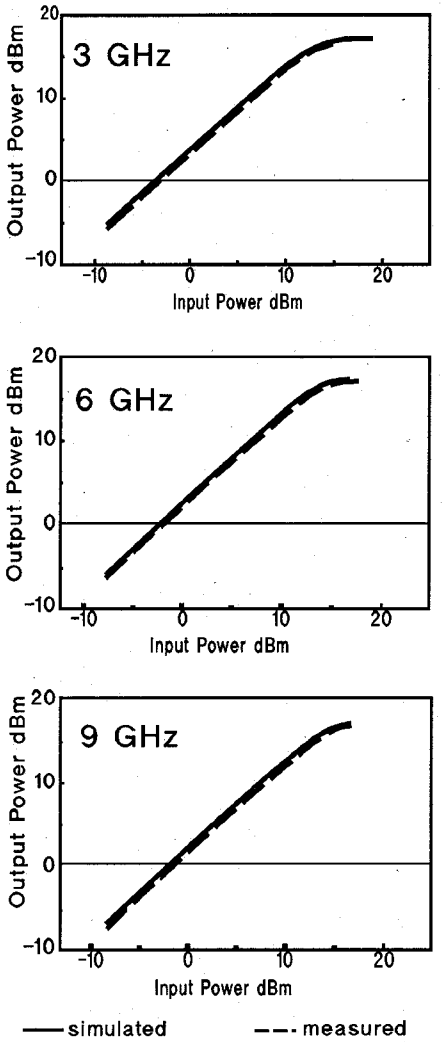


Fig. 14. Large-signal power-transfer characteristics of a 1 micron gate length MESFET (—— simulated, ---- measured data).

quasi-static approximation for use below 30 GHz and does not provide any insight into the physical behavior of the device. A key aspect of the quasi-static approach used here is that the model obeys charge-conservation since it is derived using the physical model (see [2] for details).

Fig. 14 shows that power transfer characteristics of a 1 micron gate length ion-implanted MESFET at 3, 6, and 9 GHz. The comparison between measured and simulated data is creditable for all three cases demonstrating not only the large-signal capability of this model, but also its intrinsic broadband performance. The simulated results have been obtained directly from the model without any fitting of parasitics, for physical parameters specified for a typical wafer-probed device, and the nominal 0.6 dB discrepancy can be reduced by fitting. The measured data was obtained using an automated load-pull test set.

IV. Conclusion

The physical model used in this work offers two key advantages—it is inherently capable of representing all modes of operation (dc, small- and large-signal microwave operation) and offers a uniquely accurate predictive capability for a wide range of MESFET's. This paper describes important new developments in the model and demonstrates its application and accuracy for different types of MESFET, including double-recessed power FET's. The strong dependence of breakdown voltage on gate-offset and recess depth has been demonstrated both experimentally and theoretically.

This approach offers a highly efficient means of assessing the influence of process variations on dc and microwave device performance. It has the particular advantage over equivalent circuit models in that this method can be used to predict these variations prior to fabrication and test.

Acknowledgment

The authors would like to acknowledge C. Varmazis, J. P. Lanteri, Y-H Yun and L. Ward of M/A-COM for providing measured data and for helpful discussions. Christopher Snowden is particularly grateful to M/A-COM for their support and interest during a sabbatical year spent with the Corporate Research and Development Center.

References

[1] C. M. Snowden and R. R. Pantoja, "Quasi-two-dimensional MESFET simulations for CAD," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1564–1574, Sept. 1989.

[2] R. R. Pantoja, M. J. Howes, J. R. Richardson, and C. M. Snowden, "A large-signal physical MESFET model for computer-aided design and its applications," *IEEE Trans. Microwave Theory Tech.*, vol. 37, no. 12, pp. 2039–2045, Dec. 1989.

[3] G. Ghione, C. U. Naldi and F. Filicori, "Physical modeling of GaAs MESFET's in an integrated CAD environment: From device technology to microwave circuit performance," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 457–468, Mar. 1989.

[4] F. Heliodore, M. Lefebvre, G. Salmer, and O. El-Sayed, "Two-dimensional simulation of submicrometer GaAs MESFET's: Surface effects and optimization of recessed gate structures," *IEEE Trans. Electron Devices*, vol. 35, pp. 824–830, July 1988.

[5] B. Carnez, A. Cappy, A. Kaszynski, E. Constant, and G. Salmer, "Modelling of a submicrometer gate field-effect transistor including effects of nonstationary electron dynamics," *J. Appl. Phys.*, vol. 51, pp. 784–790, Jan. 1980.

[6] P. A. Sandborn, J. R. East, and G. I. Haddad, "Quasi-two-dimensional modeling of GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. 34, pp. 985–991, May 1987.

[7] R. B. Darling, "Generalized gradual channel modeling of field-effect transistors," *IEEE Trans. Electron Devices*, vol. 35, pp. 2302–2314, Dec. 1988.

[8] C. Licqurish, M. J. Howes, and C. M. Snowden, "A new model for the dual-gate GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1497–1505, Oct. 1989.

[9] C. M. Snowden, M. J. Howes, and D. V. Morgan, "Large-signal modelling of GaAs MESFET operation," vol. ED-30, no. 12, pp. 1817–1824, Dec. 1983.

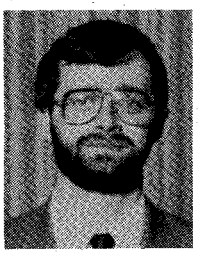
[10] M. Hines, "Dynatemp," Hines Consulting Services, MA., 1990.

[11] P. H. Ladbrooke and S. R. Blight, "Low-field low frequency dispersion of transconductance in GaAs MESFETs," *GEC Journal of Research*, vol. 5, no. 4, pp. 217–225, 1987.

[12] K. Horio, H. Yanai, and T. Ikoma, "Numerical simulation of GaAs MESFET's on the semi-insulating substrate compensated by deep traps," *IEEE Trans. Electron Devices*, vol. 35, pp. 1778–1785, Nov. 1988.

[13] T. M. Barton and C. M. Snowden, "Two-dimensional numerical simulation of trapping phenomena in the substrate of GaAs MESFET's," *IEEE Trans. Electron Devices*, June 1990.

[14] M. S. Shur and L. F. Eastman, "I-V Characteristics of GaAs MESFET with nonuniform doping profiles," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 455–461, Feb. 1980.
[15] J. M. Golio, R. J. Trew, G. N. Maracas, and H. Lefevre, "A modeling technique for characterizing ion-implanted material using *C-V* and DLTS data," *Solid-State Electron.*, vol. 27, no. 4, pp. 367–373, 1984.
[16] M. Reiser, "A two-dimensional numerical FET model for DC, AC and large-signal analysis," *IEEE Trans. Electron Devices*, vol. ED-20, pp. 35–45, 1973.
[17] Y. Wada and M. Tomizawa, "Drain avalanche breakdown in gallium arsenide MESFET's," *IEEE Trans. Electron Devices*, vol. 35, pp. 1765–1770, Nov. 1988.



Christopher M. Snowden (S'82–M'82–SM'91) received the B.S., M.Sc. and Ph.D. degrees from the University of Leeds.

After graduating in 1977 he worked as an Applications Engineer for Mullard, Mitcham. His Ph.D. studies were conducted in association with Racal-MESL and were concerned with the large-signal characterization of MESFET oscillators. In 1982 he was appointed Lecturer in the Department of Electronics at the University of York. He joined the Microwave Solid State Group in the Department of Electronic and Electrical Engineering at the University of Leeds in 1983, where he is a Senior Lecturer. During 1987 he was a Visiting Research Associate at the California Institute of Technology. He has been a Consultant to M/A-COM Inc., Corporate Research and Development since 1989, where he was on sabbatical leave during the period 1990–91. He is a Member of the MIT Electromagnetics Academy. His main research interests include semiconductor device modelling, nonlinear subsystem design, CAD and characterization, and advanced semiconductor devices.

Dr. Snowden has written five books and over 90 papers, and is on the editorial board of several journals. He is a Member of the IEE and serves on the Microwave Devices and Techniques Committee. He also serves on the IEEE MTT-1 CAD Sub-Committee. In addition, he is a founding member of the International GaAs Simulation Group.

Renato Pantoja was born in Rio de Janeiro, Brazil on March 14th, 1961. He received the B.Sc. and M.Sc. degrees from the Military Engineering Institute in 1983 and 1986, respectively.

After graduating he worked as a Research Assistant at the Military Engineering Institute on the development of broad-band microwave voltage-controlled oscillators and antennas. He joined the Microwave Solid State Group at Leeds University, UK in 1986 and graduated with a Ph.D. in 1990. After completing his Ph.D. he held a Research Fellowship at Leeds on Physical Modelling for Non-Linear CAD. He is currently a member of the Corporate Research and Development Center at M/A-COM Inc., Burlington, MA. His main research interests are the non-linear characterization of MESFET's and HEMT's incorporated into large-signal circuits.